AMENDMENTS

In the Claims

The following is a marked-up version of the claims with the language that is underlined ("___") being added and the language that contains strikethrough ("~~—~~") being deleted:

1. (Currently Amended) A data converter for converting a group of vectors from a time serial to a time parallel format, wherein in the time serial format, sets of corresponding components of the vectors each have a time slot, and in time parallel format, each vector has a time slot, the converter comprising:

an input rotator configured to rotate each set of corresponding components of all time serial vectors by an amount that depends on the time slot of the set of corresponding components, wherein the input rotator is comprised of a plurality of multiplexer stages for rotating ~~the~~ each set of corresponding components;

a bank of register files coupled to the input rotator to receive ~~the~~ a rotated set of corresponding components, and having a register file in the bank configured to store each rotated set of corresponding components;

an output rotator coupled to the bank of registers files, for receiving and rotating the components of a vector by an amount that depends on the time slot of the vector in time parallel format to generate ~~a~~ the vector ~~having~~ in time parallel format, wherein the output rotator is comprised of a plurality of multiplexer stages for rotating the components of each vector; and

a controller configured to control ~~the~~ addressing of the bank of register files when the corresponding components of each vector are stored in a register of the bank in horizontal and vertical write operations, and to control ~~the~~ addressing of the bank to collect the components of each vector for subsequent output rotation in horizontal and vertical read operations, said controller further configured to control alternating horizontal reading and writing and vertical

reading and writing operations upon the bank of register files, wherein the controller is comprised of:

address lines configured to identify ~~the~~ a proper component register of each respective register bank, wherein the address lines are provided by outputs of multiplexers configured to receive inputs from an up counter and a down counter located within the controller; and

control bits configured to control ~~the~~ operation of the multiplexer stages within the input rotator and the output rotator, wherein the control bits are provided by outputs from the up counter.

2. (Original) The data converter of claim 1,

wherein each vector has n components indexed from 0 to n-1 such that there are 0 to n-1 sets of corresponding components; and

wherein the amount of rotation by the input rotator is zero for the 0^{th} set of corresponding components, and n-1 steps clockwise for the (n-1)th set, any intervening sets of corresponding components being rotated by an amount equal to the ordinal number of the set.

3. (Original) The data converter of claim 1,

wherein there are n vectors indexed from 0 to n-1; and

wherein the amount of rotation by the output rotator is zero for the 0^{th} vector and n-1 steps counter-clockwise for the (n-1)th vector, any intervening vectors being rotated by an amount equal to the ordinal number of the vector.

4. (Currently Amended) The data converter of claim 1, wherein each register file in the bank includes a register for storing ~~the~~ vector components.

5. (Original) The data converter of claim 4, wherein each vector has n components and each register file in the bank has n component registers.

6. (Original) The data converter of claim 5, wherein there are n register files in the bank.

7. (Currently Amended) The data converter of claim 1, wherein the bank of register files is configured to write and read ~~the~~ vector components at the same clock cycle.

8. (Canceled)

9. (Currently Amended) The data converter of claim 1, wherein ~~the~~ each vector has n components and the controller horizontally writes n sets of corresponding components and horizontally reads n vectors.

10. (Original) The data converter of claim 9, wherein, after the controller horizontally writes n sets of corresponding components and horizontally reads n vectors, the controller vertically writes n sets of corresponding components and vertically reads n vectors.

11. (Currently Amended) The data converter of claim 1, wherein the output rotator rotates ~~the~~ each vector component a position equal and opposite to the input rotator.

12-17. (Canceled)

18. (Currently Amended) A data converter for converting a group of vectors from a time serial to a time parallel format, wherein in the time serial format, sets of corresponding

components of the vectors each have a time slot, and in time parallel format, each vector has a time slot, the converter comprising:

input rotation means for rotating each set of corresponding components of all vectors by a first prescribed amount depending on the particular set, wherein the input rotation means is comprised of a plurality of multiplexing means for rotating ~~the~~ each set of corresponding components;

storage means coupled to the input rotation means, for storing ~~the~~ each rotated set of corresponding components; and

output rotation means coupled to the storage means, for receiving components of a vector from the storage means and rotating the components of the vector by a second prescribed amount depending on the particular vector to generate a vector in time parallel format, wherein the output rotation means is comprised of a plurality of multiplexing means for rotating the ~~corresponding~~ components of each vector; and

controller means, communicably coupled to the input ~~rotator~~ rotation means, the storage means and the output ~~rotator~~ rotation means, for controlling ~~the~~ writing and reading of ~~the~~ vector components to the storage means and the rotation of the vector components by the output rotation means and the input rotation means, and for controlling said reading and writing operations horizontally and vertically, said horizontal operations alternating with said vertical operations, wherein the input ~~rotator~~ rotation means and the output ~~rotator~~ rotation means are communicably coupled to the controller means through control signals, wherein the control signals between the controller means and input ~~rotator~~ rotation means are the same control signals as the control signals between the controller and the output ~~rotator~~ rotation means, and wherein the controller means is comprised of:

address lines configured to identify ~~the~~ a proper component register of each respective register bank, wherein the address lines are provided by outputs of

multiplexers configured to receive inputs from an up counter and a down counter located within the controller; and

control bits configured to control ~~the~~ operation of the multiplexer stages within the input ~~rotator~~ rotation and the output rotator, wherein the control bits are provided by outputs from the up counter.

19. (Currently Amended) The data converter of claim 18 wherein:

the input rotation means is an input rotator configured to rotate each set of corresponding components of all vectors by an amount that depends on the time slot of the set of corresponding components;

the storage means is a bank of register files with a register file in the bank configured to store each rotated set of corresponding components; and

the output rotation means is an output rotator configured to receive and rotate the components of a vector by an amount that depends on the time slot of the vector.

20. (Currently Amended) The data converter of claim 19 wherein the storage means is configured to write and read ~~the~~ vector components in the same clock cycle.

21. (Original) The data converter of claim 20 wherein the storage means is configured to write corresponding components horizontally and then read vectors horizontally over a prescribed number of clock cycles.

22. (Original) The data converter of claim 21, wherein, during another prescribed number of clock cycles, the storage means is configured to write corresponding components vertically and then read vectors vertically.

23 – 24. (Canceled)

25. (Original) The data converter of claim 18 wherein the output rotation means rotates time parallel vector components in a direction opposite to the direction that the input rotation means rotates a set of corresponding vector components.